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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/699,221	Confirmation No.:	2799
First Named Inventor:	Constantin Bulucea	Filing Date:	31 October 2003
Group Art Unit:	2891	Examiner:	Farahani, D.
Atty. Docket No.:	NS-5127-1D US		
Title:	Design and Operation of Gate-enhanced Junction Varactor With Gradual Capacitance Variation		
Assignee:	National Semiconductor Corporation		

Mountain View, California
12 April 2006

COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE OF CERTAIN CLAIMS

Sir:

The following comments are presented on the statement of the reasons for the allowance of independent Claim 61 and its dependent claims, Nos. 62 - 82, as given in the Notice of Allowability mailed 3 January 2006 for the above patent application. Claim 61 is repeated below:

61. A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurring in the body region and occupying a lateral inversion area along the primary surface, the inversion area reaching a maximum value when the inversion layer is fully present, the

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

varactor having a maximum capacitance dependent on the maximum inversion area in combination with the plate area, the plate electrode being at a plate-to-body voltage relative to the body electrode, the gate electrode being at a gate-to-body voltage relative to the body electrode, the inversion layer comprising multiple variably appearing inversion portions respectively characterized by corresponding different zero-point threshold voltages of like sign, each inversion portion appearing/disappearing when the gate-to-body voltage passes through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero, each inversion portion meeting the plate region or/and being continuous with the another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that inversion portion; and

adjusting the plate and maximum inversion areas to control the maximum and minimum capacitances of the varactor.

On page 2, the Notice of Allowability states that "The reason for allowance of claims 61 - 82 is the inclusion therein of the limitation that of the varactor having a semiconductor island, as defined in claim 61, along with the other limitations in those claims". While each of independent Claims 83, 89, and 95 recites "a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions", Claim 61 does not recite anything that reasonably constitutes a "semiconductor island", i.e., a semiconductor region laterally surrounded by isolating material such as electrically insulating material. The same applies to dependent Claims 62 - 82. The reasons presented in the Notice of Allowability for allowing Claims 61 - 82 do not appear on point.

Claim 61 is generally a method analog of allowed independent Claim 1 of parent U.S. patent application 10/054,653. Both Claim 61 and Claim 1 of the parent application recite that an inversion layer in the body region below the gate electrode comprises "multiple variably appearing inversion portions respectively characterized by corresponding different zero-point threshold voltages of like sign, each inversion portion appearing/disappearing when the gate-to-body voltage passes through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero".

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
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Fax: 650-964-9779

The Notice of Allowability mailed 18 October 2005 for the parent application specifies on page 4 that the reason for allowing Claims 1 - 33 of the parent application is the inclusion therein of "A varactor having an inversion layer, which variably appears and disappears below the gate electrode". Applicant's Attorney interprets this language from the

parent's Notice of Allowability to mean that the inversion layer is situated below the gate electrode and comprises multiple portions which variably appear and disappear (below the gate electrode). Since present Claim 61 and parent Claim 1 both recite such a multi-portion inversion layer and since the reason stated in the parent's Notice of Allowability for allowing parent Claim 1 is the inclusion of the multi-portion inversion layer, present Claim 61 distinguishes the prior art of record in the above application in basically the same way that parent Claim 1 distinguishes the prior art of record in the parent application, namely in the inclusion of an inversion layer which is situated in the body region below the gate electrode and which comprises multiple portions that variably appear and disappear. The same distinction over the prior art of record in the above application applies to dependent Claims 62 - 82.

Additionally, the Notice of Allowability for the above application refers to such a multi-portion inversion layer in the reasons for allowing certain claims other than Claims 61 - 82. More particularly, the present Notice of Allowability states on page 3 that "The reason for allowance of claims 117-128 is the inclusion therein of the limitation that of varying the plate to body voltage while maintaining the gate to body voltage constant to cause multiple inversion layers in the body region, along with the other limitations in those claims". This statement from the present Notice of Allowability indicates that the Examiner recognizes that such a multi-portion inversion layer provides inventiveness and implicitly supports the preceding comments that Claims 61 - 82 distinguish the prior art or record in the above application due to the recited multi-portion inversion layer.

Inasmuch as this paper is being submitted after the issue fee was paid on the above application, simply place this paper in the PTO file for the above application.

Please telephone Applicant's Attorney at 650-964-9767 if there are any questions.

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Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicant(s)
Reg. No. 29,089

210 Central Avenue
Mountain View, CA 94043-4869

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779